FIG. 1A

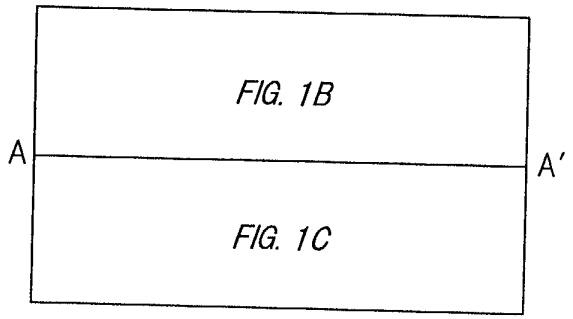
FIG. 1B
A
A'
FIG. 1C

FIG. 1B

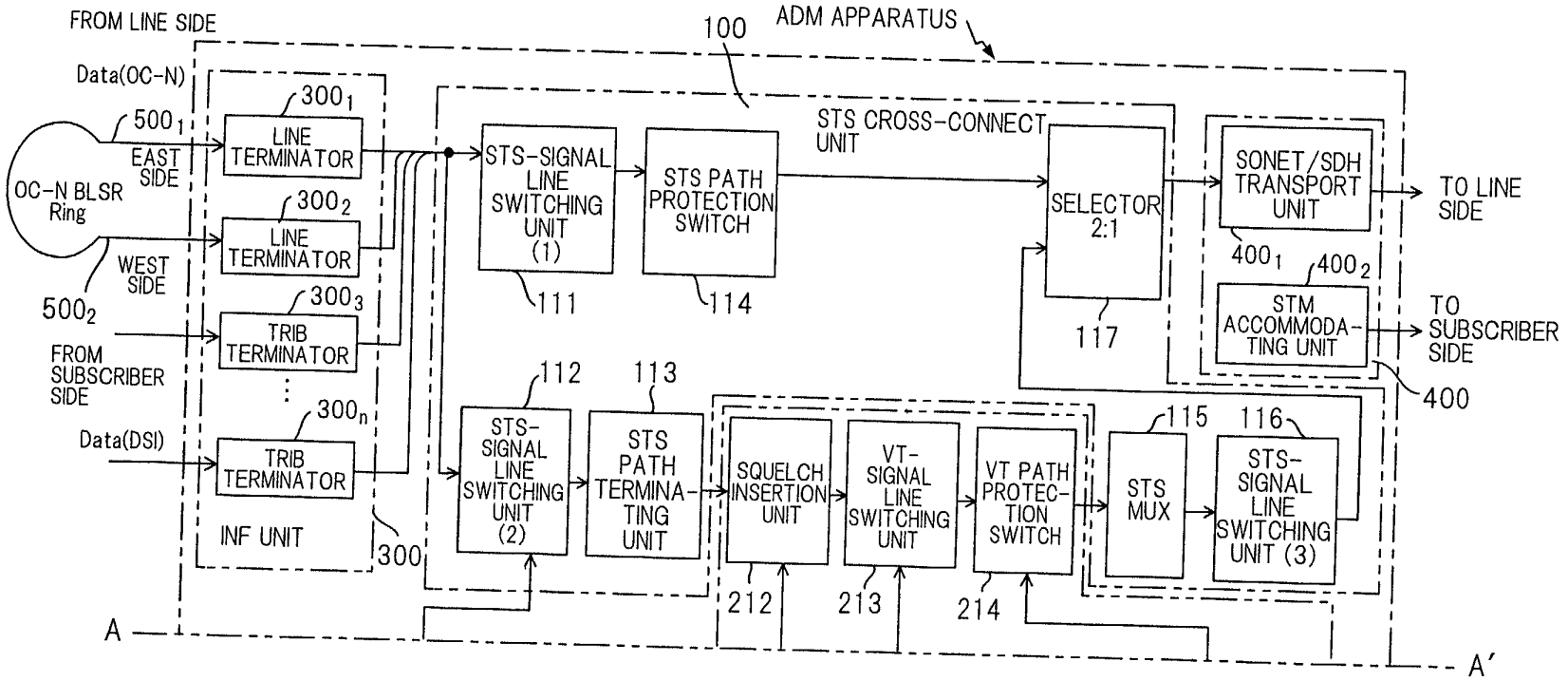
FROM LINE SIDE
Data(OC-N)
500 1
EAST SIDE
OC-N BLSR Ring
WEST SIDE
500 2
FROM SUBSCRIBER SIDE
Data(DSI)
300 1
LINE TERMINATOR
300 2
LINE TERMINATOR
300 3
TRIB TERMINATOR
300 n
TRIB TERMINATOR
INF UNIT
300
100
ADM APPARATUS
STS-SIGNAL LINE SWITCHING UNIT (1)
111
STS PATH PROTECTION SWITCH
114
STS CROSS-CONNECT UNIT
SELECTOR 2:1
117
SONET/SDH TRANSPORT UNIT
400 1
400 2
STM ACCOMMODA-TING UNIT
400
TO LINE SIDE
TO SUBSCRIBER SIDE
112
STS-SIGNAL LINE SWITCHING UNIT (2)
113
STS PATH TERMINA-TING UNIT
SQUELCH INSERTION UNIT
212
VT-SIGNAL LINE SWITCHING UNIT
213
VT PATH PROTEC-TION SWITCH
214
115
STS MUX
116
STS-SIGNAL LINE SWITCHING UNIT (3)
A
A'

FIG. 1C

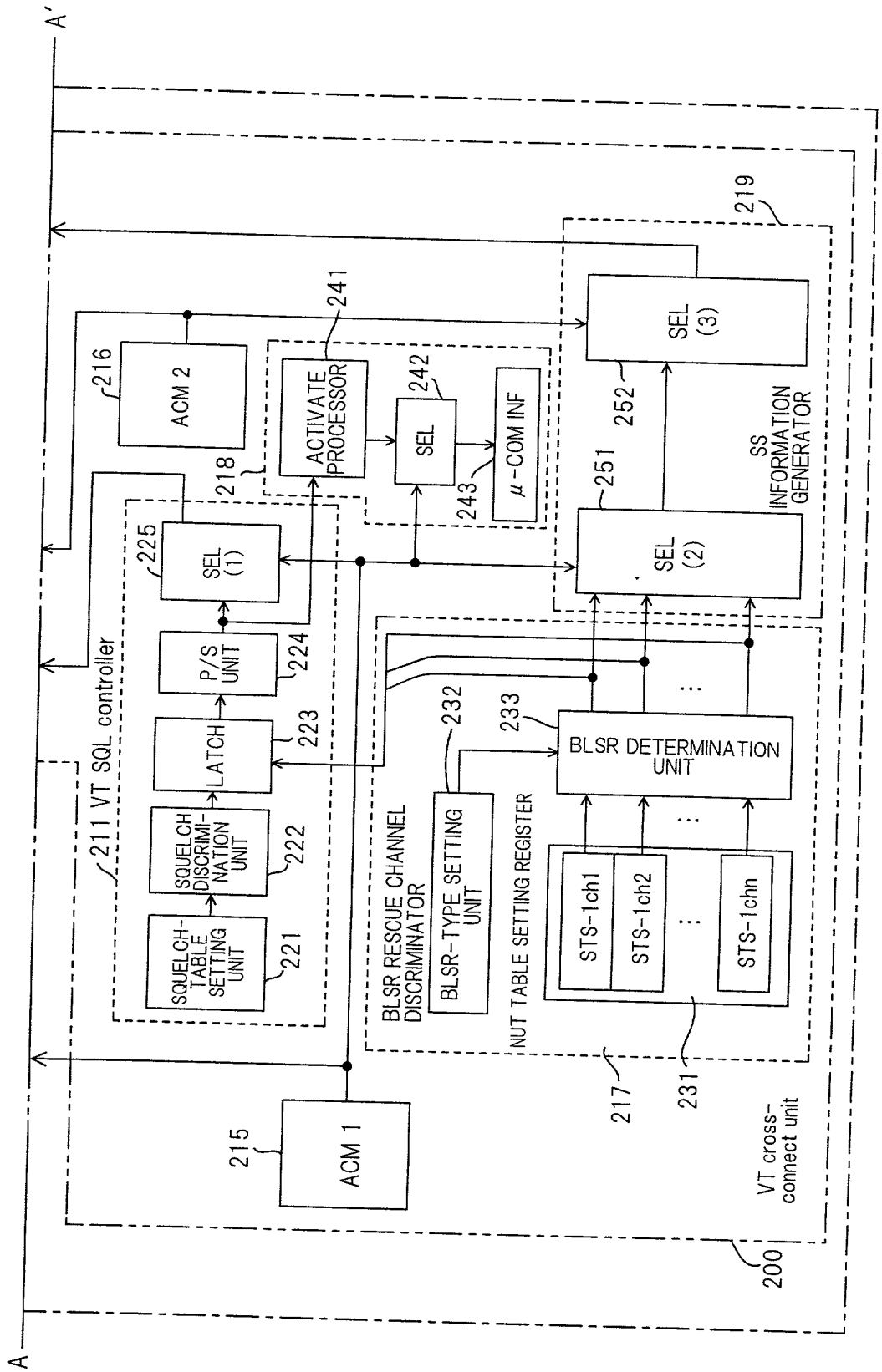
A
A'
200
VT cross-connect unit
215
ACM 1
216
ACM 2
217
231
NUT TABLE SETTING REGISTER
STS-1ch1
STS-1ch2
STS-1chn
BLSR RESCUE CHANNEL DISCRIMINATOR
BLSR-TYPE SETTING UNIT
232
233
BLSR DETERMINATION UNIT
211 VT SQL controller
SQUELCH-TABLE SETTING UNIT
221
SQUELCH DISCRIMI-NATION UNIT
222
LATCH
223
P/S UNIT
224
225
SEL (1)
218
ACTIVATE PROCESSOR
241
SEL
242
243
μ-COM INF
219
SEL (2)
SEL (3)
251
252
SS INFORMATION GENERATOR

FIG. 2

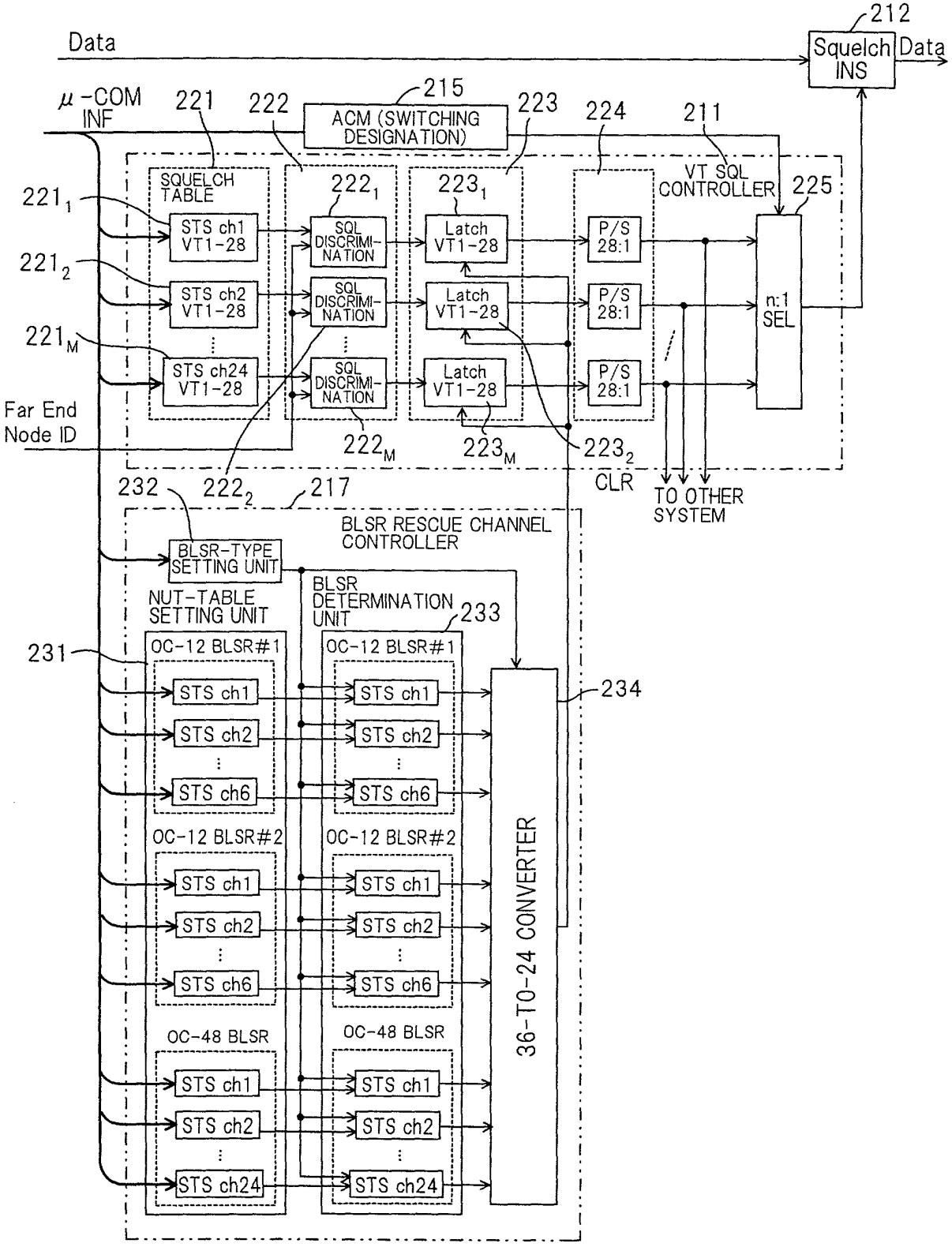
Data
212
Squelch INS
Data
μ-COM INF
221
222
215
ACM (SWITCHING DESIGNATION)
223
224
211
SQUELCH TABLE
VT SQL CONTROLLER
225
221 1
221 2
221 M
STS ch1 VT1-28
STS ch2 VT1-28
STS ch24 VT1-28
222 1
223 1
SQL DISCRIMI-NATION
Latch VT1-28
P/S 28:1
n:1 SEL
Far End Node ID
222 M
223 M
223 2
CLR
TO OTHER SYSTEM
232
222 2
217
BLSR RESCUE CHANNEL CONTROLLER
BLSR-TYPE SETTING UNIT
NUT-TABLE SETTING UNIT
BLSR DETERMINATION UNIT
233
231
OC-12 BLSR#1
OC-12 BLSR#2
OC-48 BLSR
STS ch1
STS ch2
STS ch6
STS ch24
234
36-TO-24 CONVERTER

FIG. 3A

<CONFIGURATION FOR OC-12 BLSR APPLICATION>

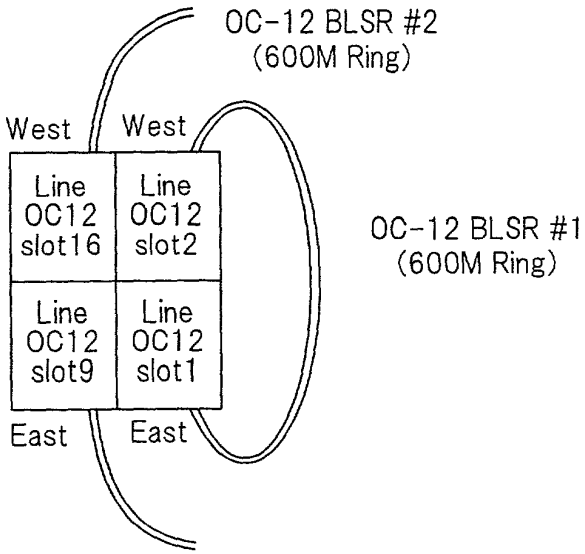

FIG. 3B

<CONFIGURATION FOR OC-48 BLSR APPLICATION>

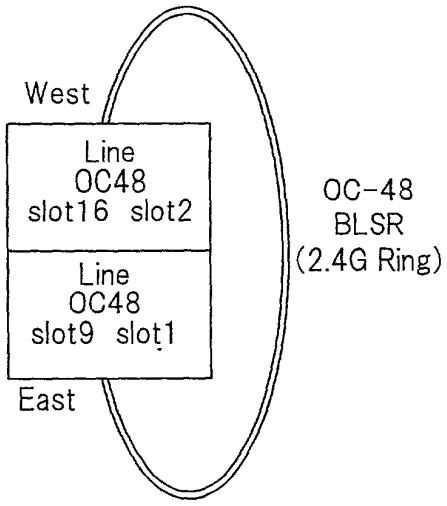

FIG. 4

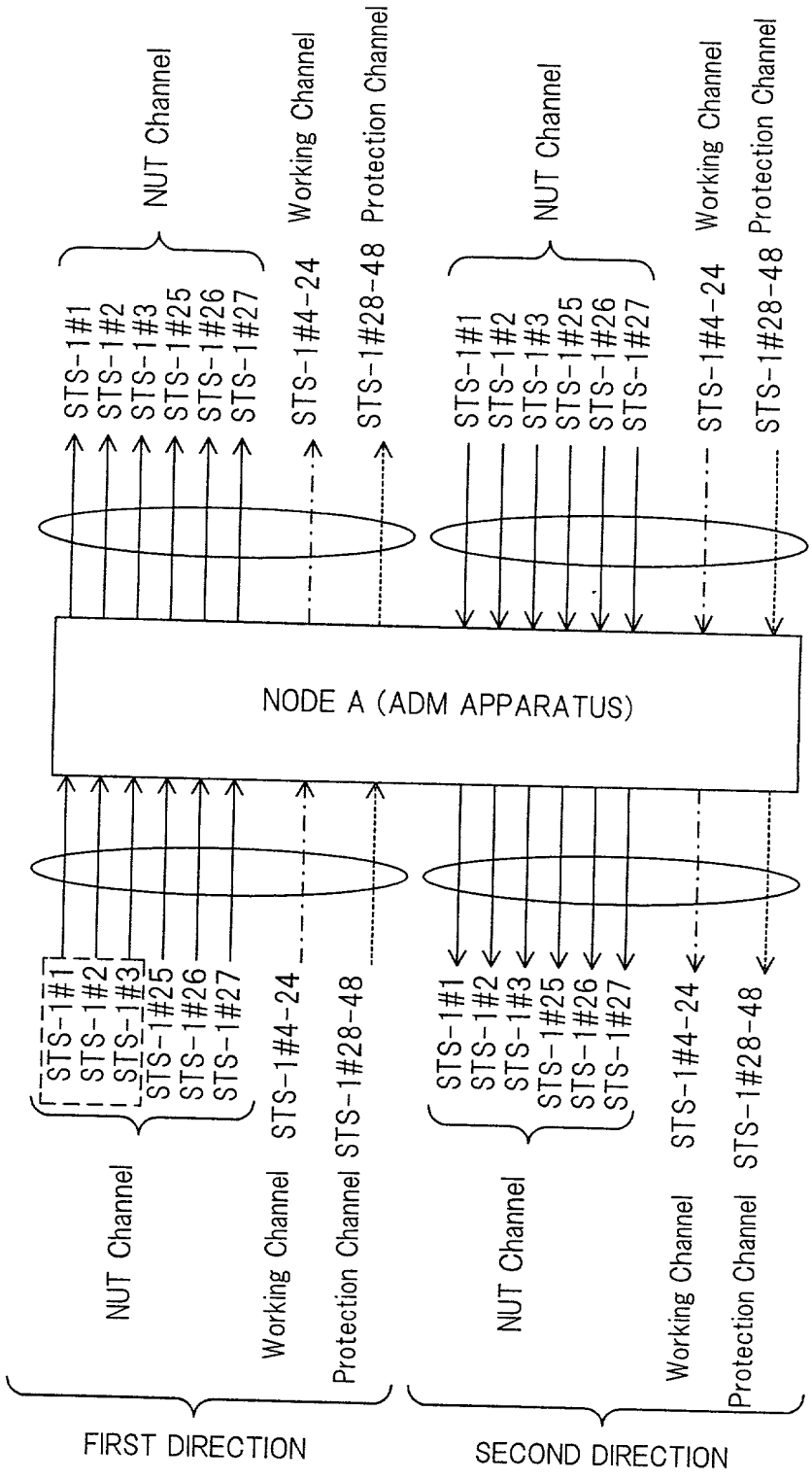
Fiber1(East)
Fiber1(WEST)
NODE A (ADM APPARATUS)
Fiber2
Fiber2
NUT Channel
STS-1#1
STS-1#2
STS-1#3
STS-1#25
STS-1#26
STS-1#27
Working Channel
STS-1#4-24
Protection Channel
STS-1#28-48
FIRST DIRECTION
SECOND DIRECTION

FIG. 5

OC-12 BLSR #1

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	ch6	ch5	ch4	ch3	ch2	ch1

OC-12 BLSR #2

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	ch6	ch5	ch4	ch3	ch2	ch1

OC-48 BLSR

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	ch12	ch11	ch10	ch9	ch8	ch7	ch6	ch5	ch4	ch3	ch2	ch1

OC-48 BLSR

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	ch24	ch23	ch22	ch21	ch20	ch19	ch18	ch17	ch16	ch15	ch14	ch13

"1"=NUT channel
"0"=not NUT channel

FIG. 6

BLSR Type		
OC12-2	OC12-1	OC-48

OC-48: OC-48 BLSR DESIGNATION; "1" : WHEN OC- 48 BLSR; "0" : NOT OC-48 BLSR
OC-12-1: OC-12 BLSR #1 DESIGNATION; "1" : WHEN OC-12 BLSR #1; "0" : NOT OC-12 BLSR #1
OC-12-2: OC-12 BLSR #2 DESIGNATION; "1": WHEN OC-12 BLSR #2; "0" : NOT OC-12 BLSR #2

FIG. 7A

APPLICATION	NUMBER OF NUT CHANNEL SETTING REGISTERS ACCORDING TO PRIOR ART (N)	NUMBER OF NUT CHANNEL SETTING REGISTERS ACCORDING TO PRESENT INVENTION (M)
not BLSR	192	0
OC-12 BLSR		6
OC-48 BLSR		24

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 7B

APPLICATION	NUMBER OF BLSR-TYPE SETTING REGISTERS ACCORDING TO PRIOR ART (N)	NUMBER OF BLSR-TYPE SETTING REGISTERS ACCORDING TO PRIOR ART (L)
WHEN OC-12 BLSR, OC-48 BLSR OR ITEM OTHER THAN BLSR CAN BE SELECTED	192	2

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 7C

APPLICATION	NUMBER OF SQL ACTIVATE PROCESSING CHANNELS ACCORDING TO PRIOR ART (NxVT*)	NUMBER OF SQL ACTIVATE PROCESSING CHANNELS ACCORDING TO PRESENT INVENTION (MxVT*)
not BLSR	5376	0
OC-12 BLSR		168 (=6×28)
OC-48 BLSR		672 (=24×28)

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 8

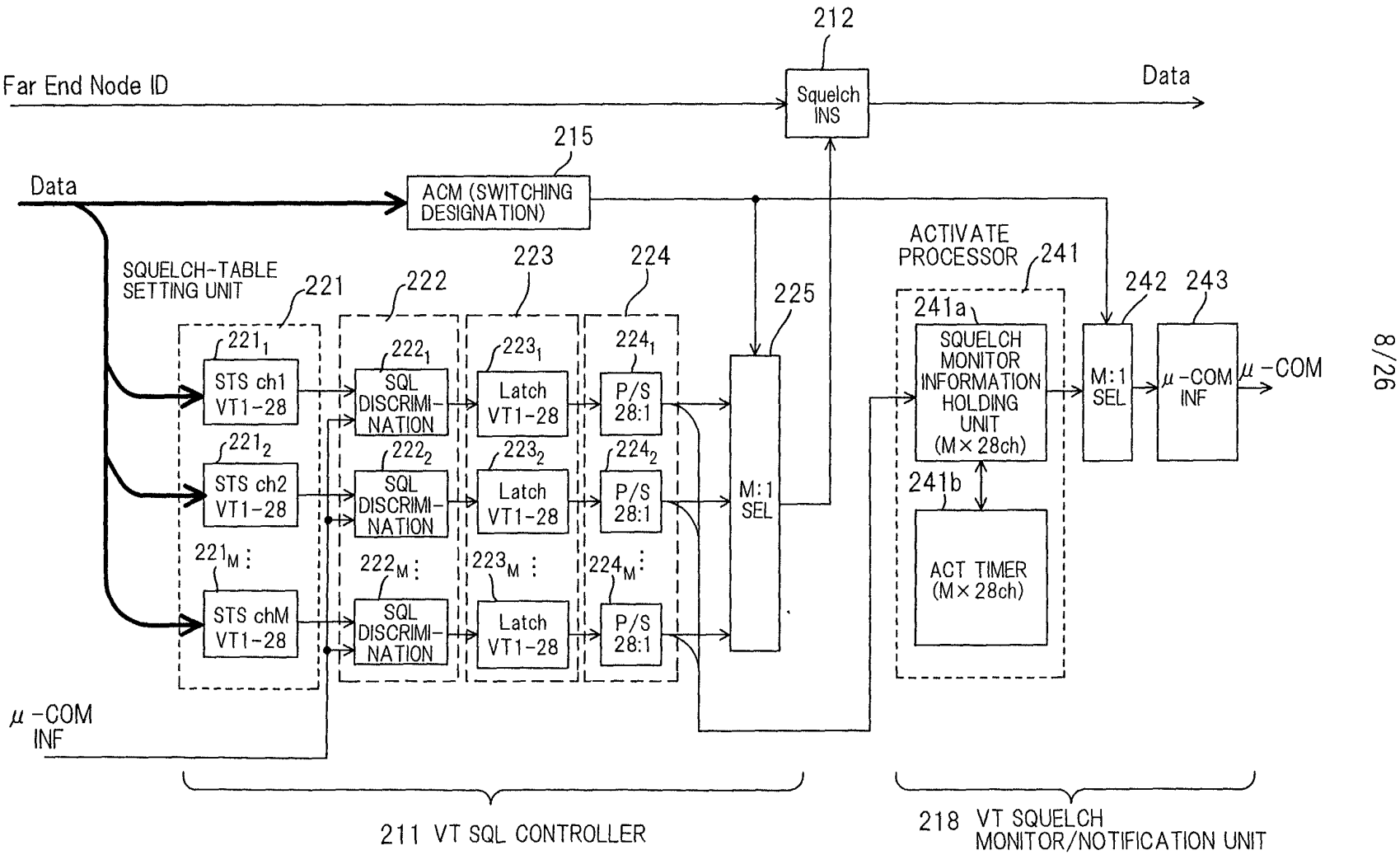
212
Far End Node ID
Squelch INS
Data
215
Data
ACM (SWITCHING DESIGNATION)
SQUELCH-TABLE SETTING UNIT
221
222
223
224
225
ACTIVATE PROCESSOR
241
241a
242
243
221_1
STS ch1 VT1-28
222_1
SQL DISCRIMI-NATION
223_1
Latch VT1-28
224_1
P/S 28:1
221_2
STS ch2 VT1-28
222_2
SQL DISCRIMI-NATION
223_2
Latch VT1-28
224_2
P/S 28:1
M:1 SEL
SQUELCH MONITOR INFORMATION HOLDING UNIT (M×28ch)
M:1 SEL
μ-COM INF
μ-COM
221_M
STS chM VT1-28
222_M
SQL DISCRIMI-NATION
223_M
Latch VT1-28
224_M
P/S 28:1
241b
ACT TIMER (M×28ch)
μ-COM INF
211 VT SQL CONTROLLER
218 VT SQUELCH MONITOR/NOTIFICATION UNIT

FIG. 9

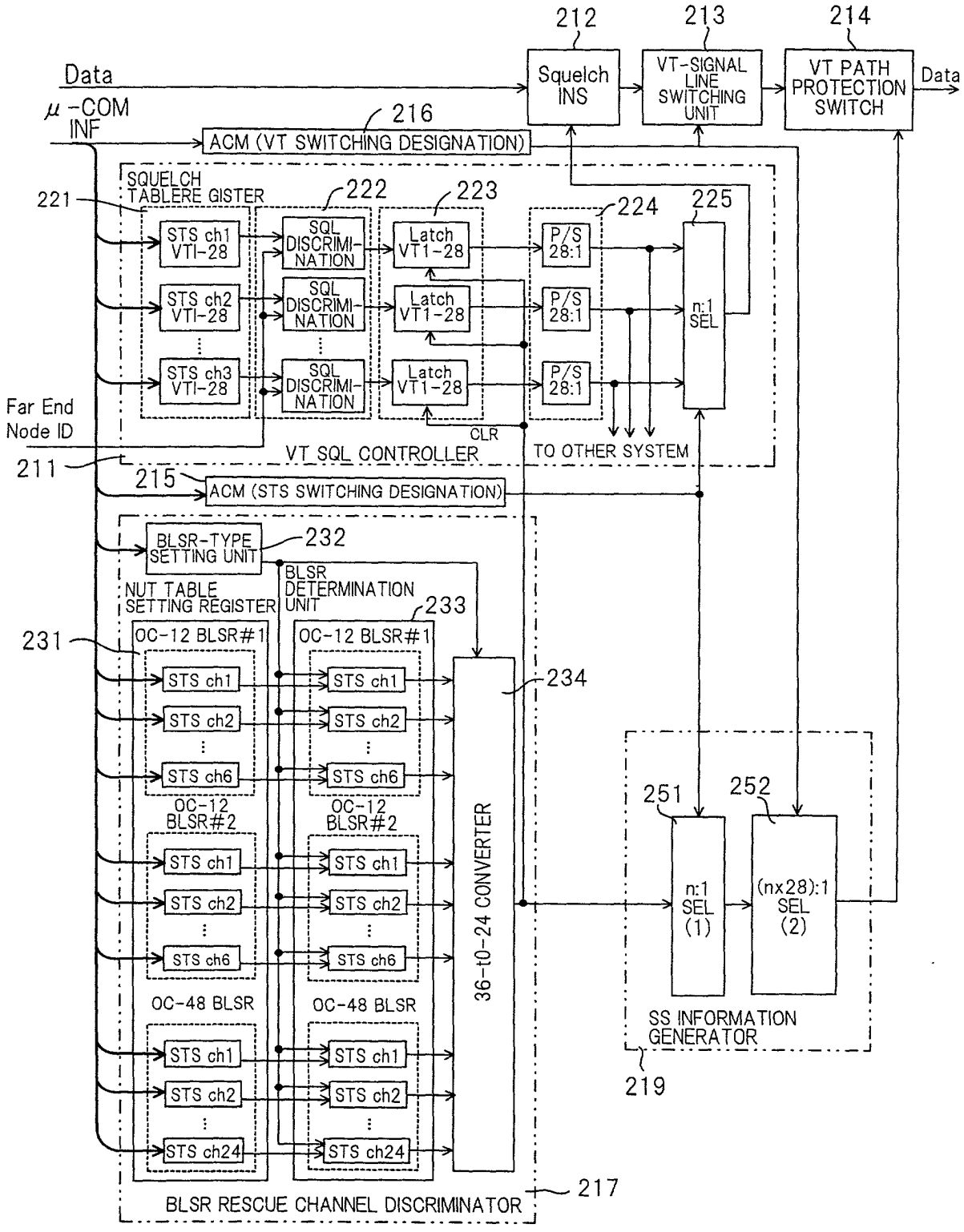
212
213
214
Squelch INS
VT-SIGNAL LINE SWITCHING UNIT
VT PATH PROTECTION SWITCH
Data
Data
μ-COM INF
216
ACM (VT SWITCHING DESIGNATION)
SQUELCH TABLERE GISTER
221
222
223
224
225
STS ch1 VTI-28
STS ch2 VTI-28
STS ch3 VTI-28
SQL DISCRIMI-NATION
Latch VT1-28
P/S 28:1
n:1 SEL
CLR
Far End Node ID
VT SQL CONTROLLER
TO OTHER SYSTEM
211
215
ACM (STS SWITCHING DESIGNATION)
BLSR-TYPE SETTING UNIT
232
BLSR DETERMINATION UNIT
NUT TABLE SETTING REGISTER
233
231
OC-12 BLSR#1
OC-12 BLSR#2
OC-48 BLSR
STS ch1
STS ch2
STS ch6
STS ch24
234
36-t0-24 CONVERTER
251
252
n:1 SEL (1)
(nx28):1 SEL (2)
SS INFORMATION GENERATOR
219
BLSR RESCUE CHANNEL DISCRIMINATOR
217

FIG. 10

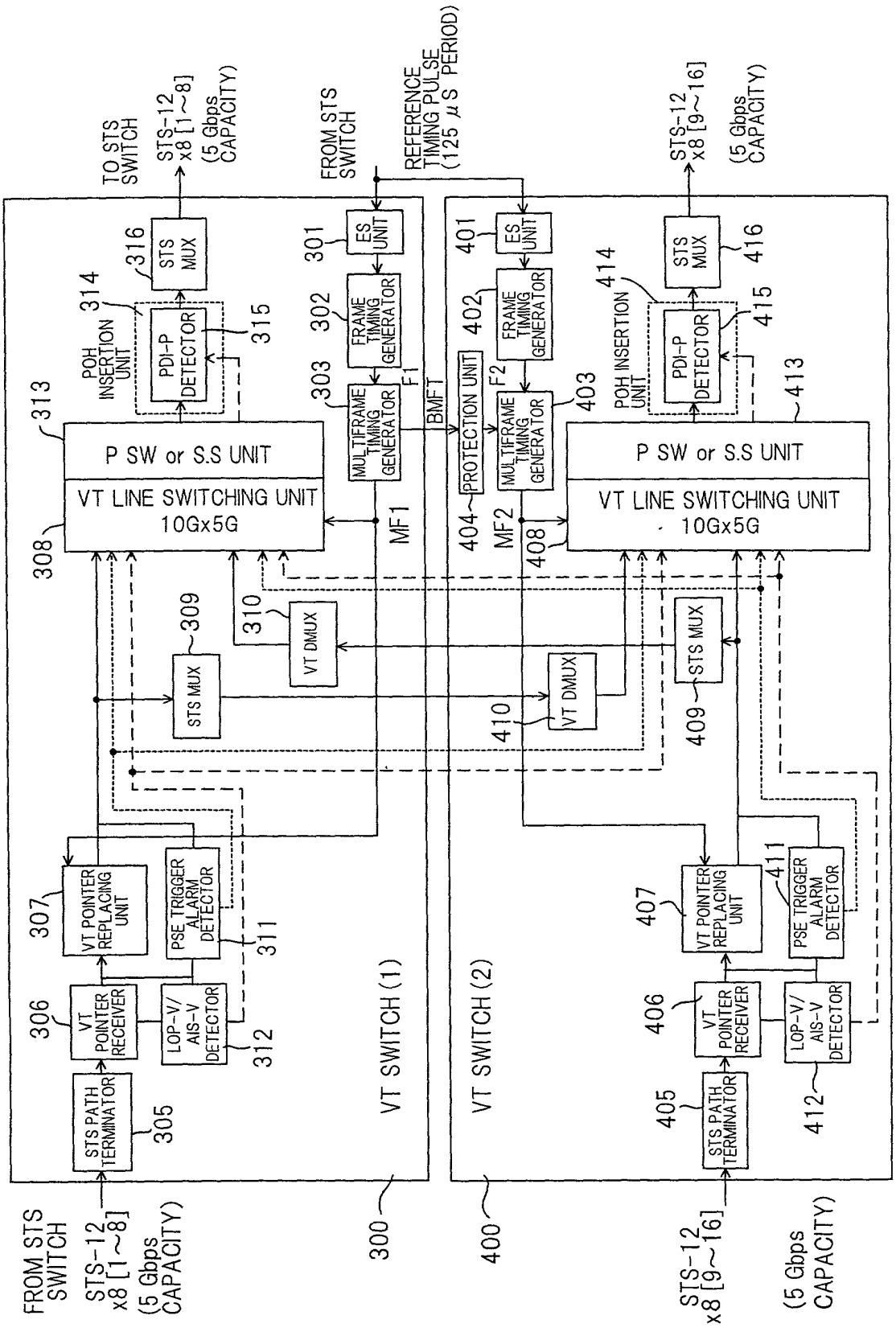
FROM STS SWITCH
STS-12 x8 [1~8]
(5 Gbps CAPACITY)
STS-12 x8 [9~16]
(5 Gbps CAPACITY)
TO STS SWITCH
STS-12 x8 [1~8]
(5 Gbps CAPACITY)
FROM STS SWITCH
REFERENCE TIMING PULSE (125 μS PERIOD)
STS-12 x8 [9~16]
(5 Gbps CAPACITY)
VT SWITCH (1)
VT SWITCH (2)
300
400
P SW or S.S UNIT
VT LINE SWITCHING UNIT 10Gx5G
308
313
MF1
MF2
BMFT
F1
F2
STS PATH TERMINATOR
305
405
VT POINTER RECEIVER
306
406
LOP-V/ AIS-V DETECTOR
312
412
VT POINTER REPLACING UNIT
307
407
PSE TRIGGER ALARM DETECTOR
311
411
STS MUX
309
409
VT DMUX
310
410
POH INSERTION UNIT
314
414
PDI-P DETECTOR
315
415
STS MUX
316
416
ES UNIT
301
401
FRAME TIMING GENERATOR
302
402
MULTIFRAME TIMING GENERATOR
303
403
PROTECTION UNIT
404
408

FIG. 11

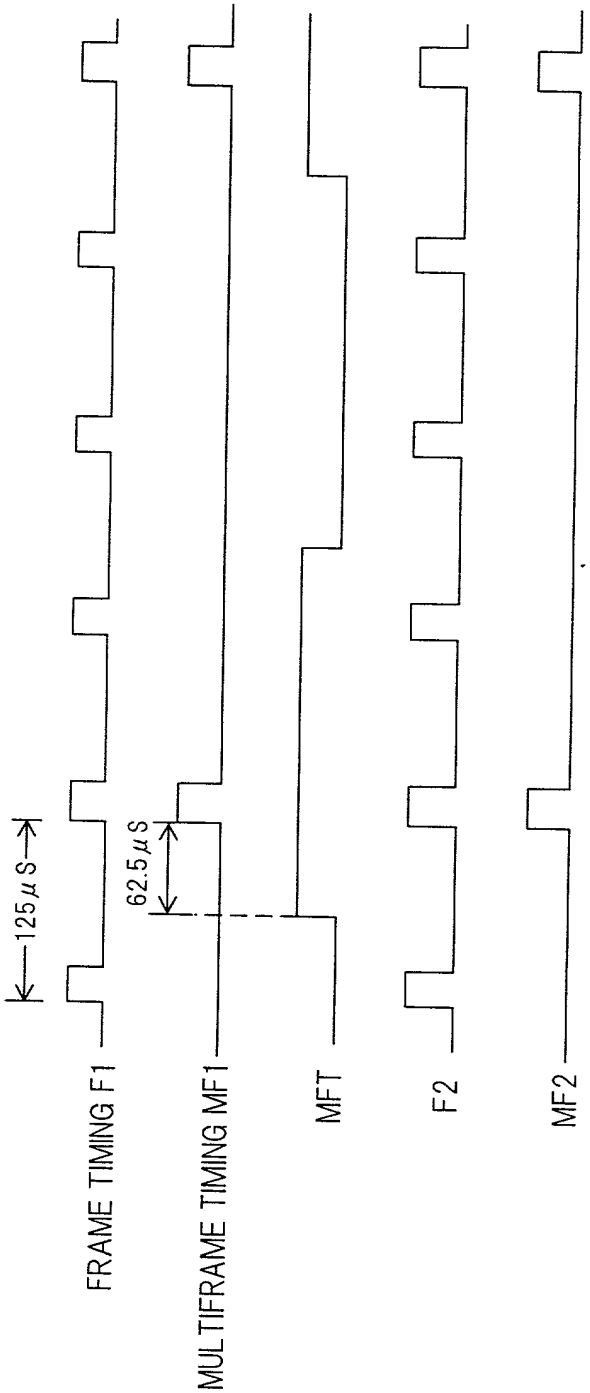
125μS
62.5μS
FRAME TIMING F1
MULTIFRAME TIMING MF1
MFT
F2
MF2

FIG. 12 PRIOR ART

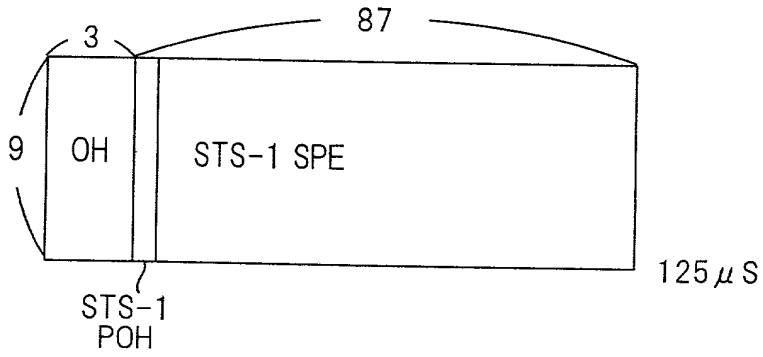

FIG. 13 PRIOR ART

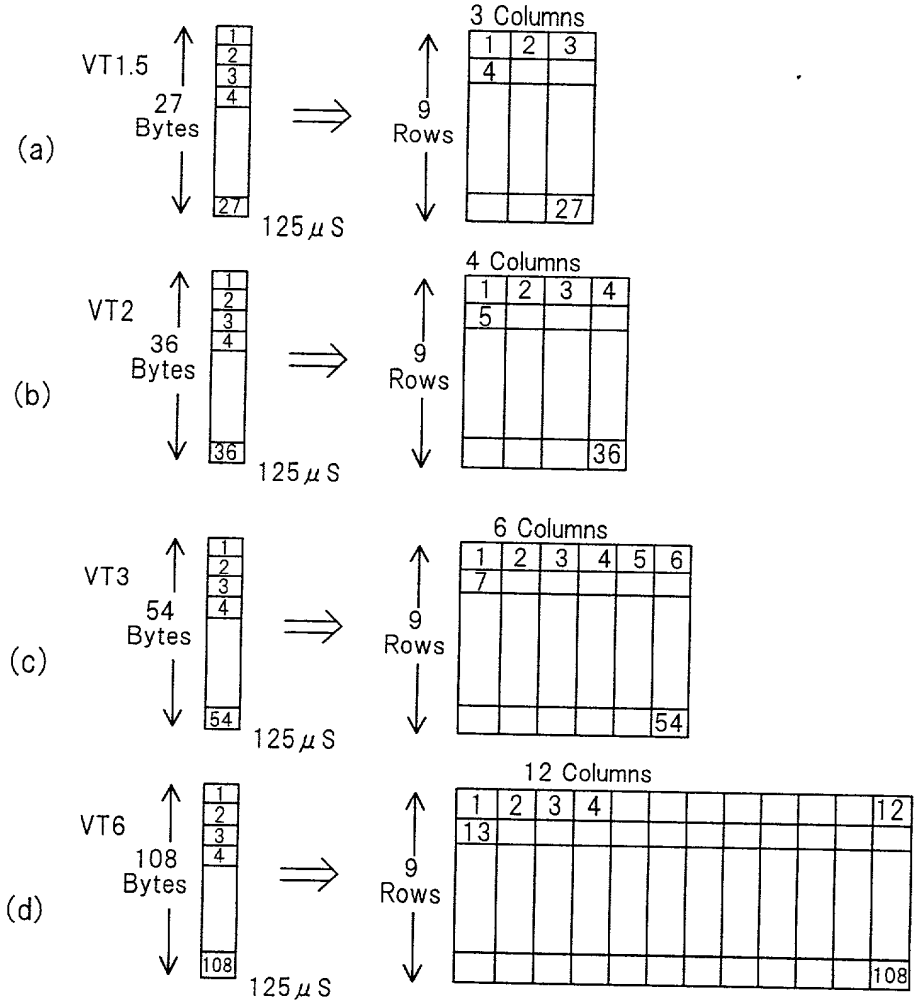

FIG. 14 PRIOR ART

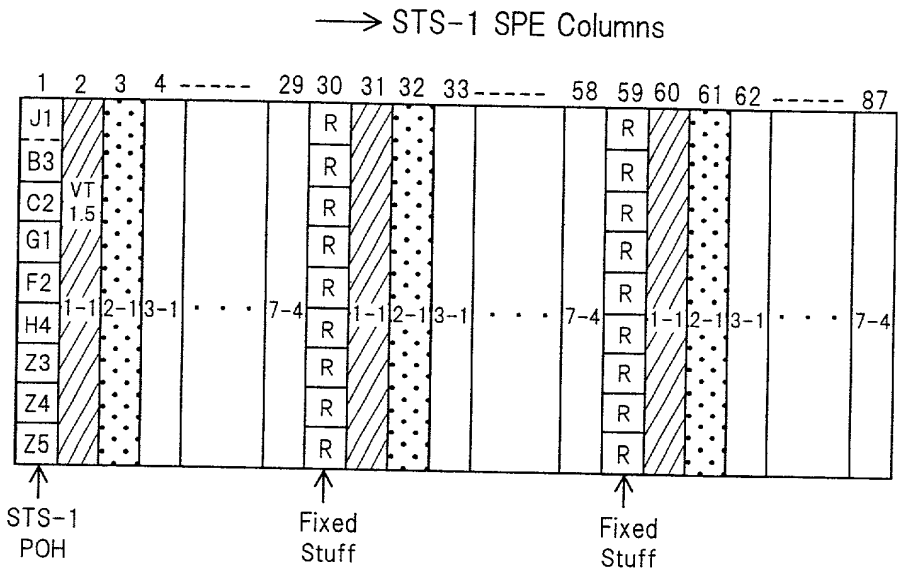

FIG. 15 PRIOR ART

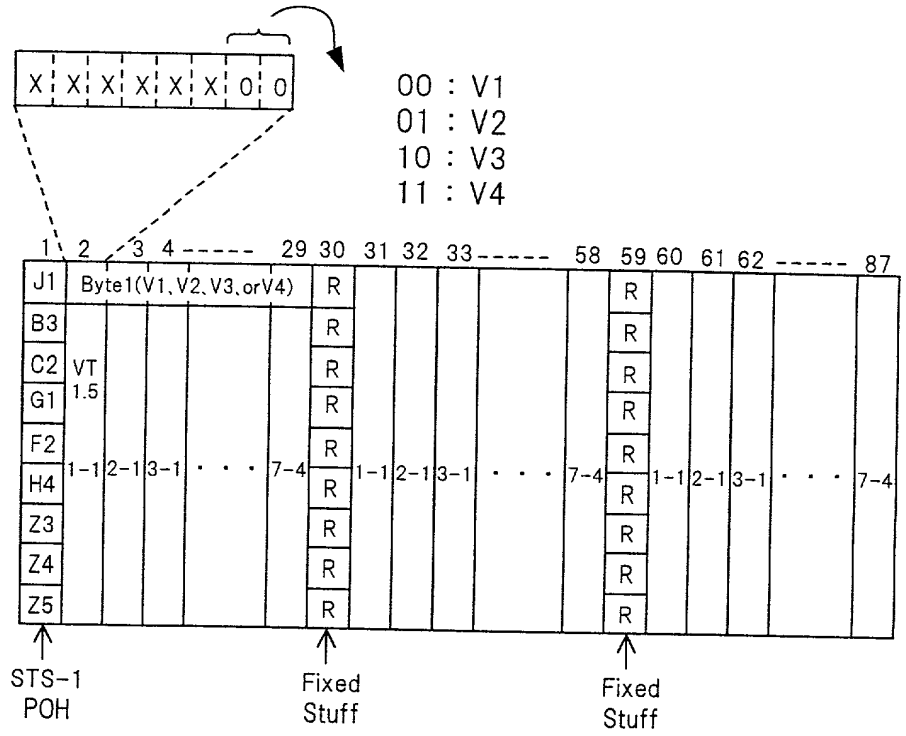

FIG. 16A PRIOR ART

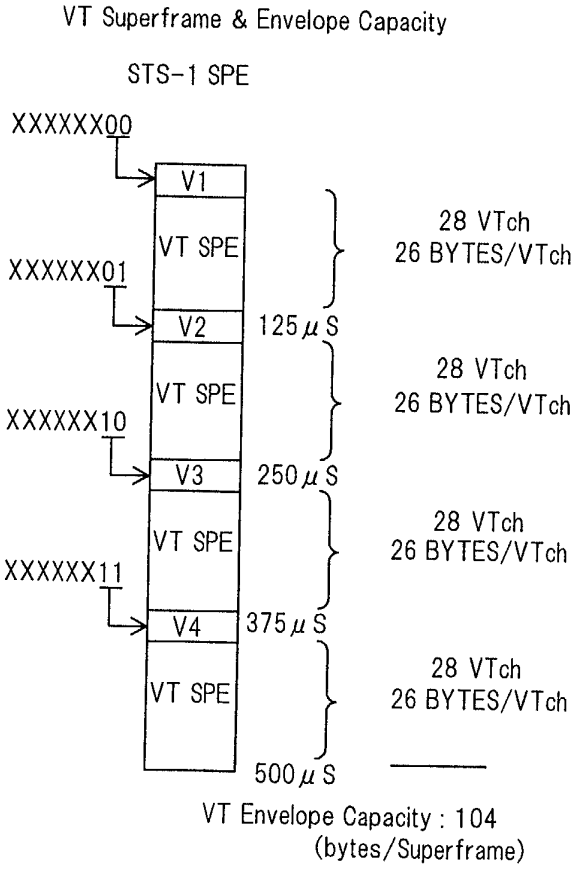

FIG. 16B PRIOR ART

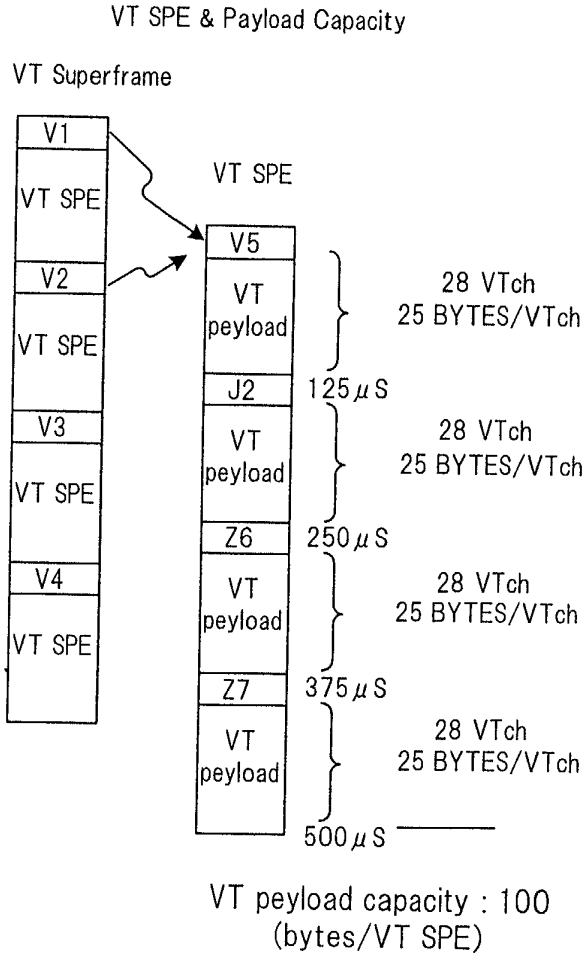

FIG. 17 PRIOR ART

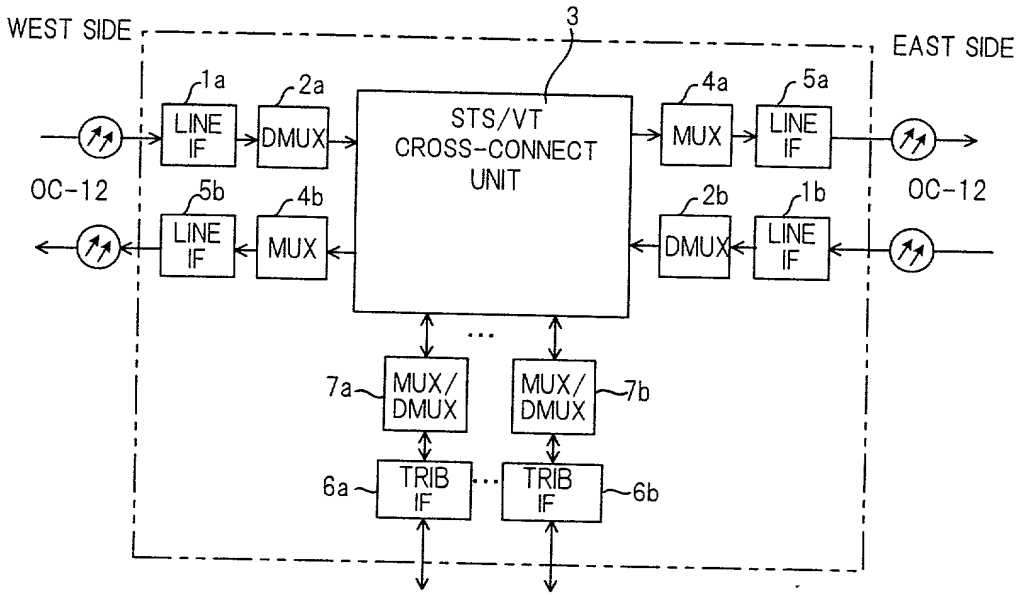

FIG. 18 PRIOR ART

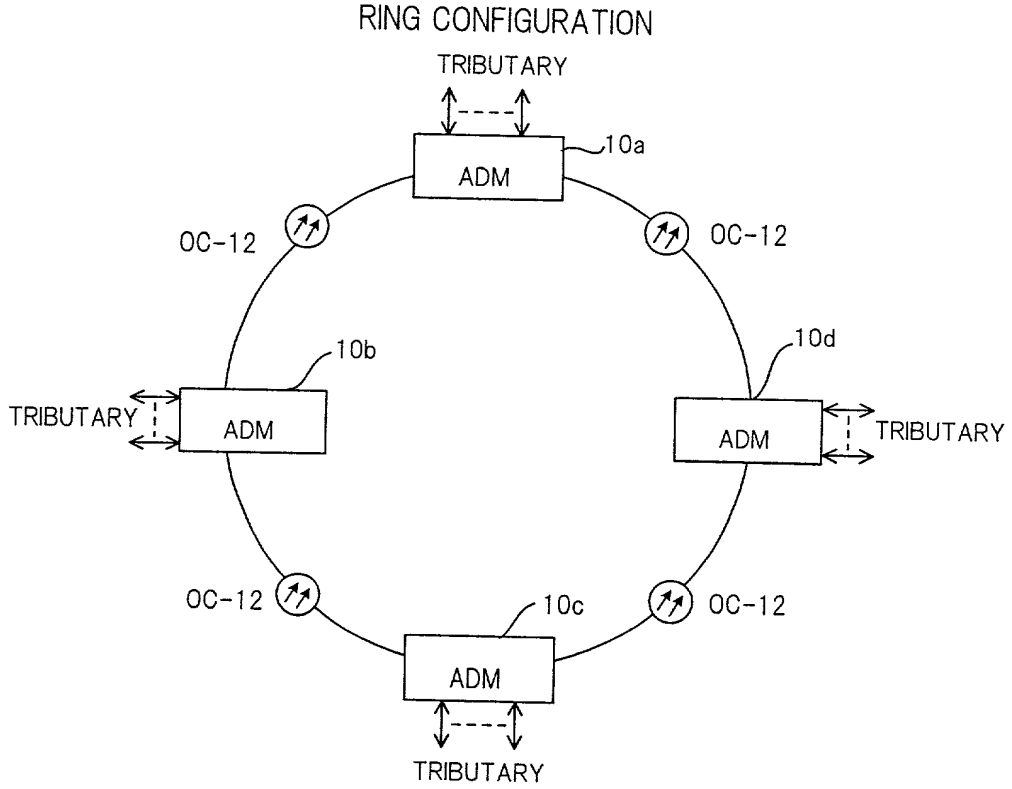

FIG. 19 PRIOR ART

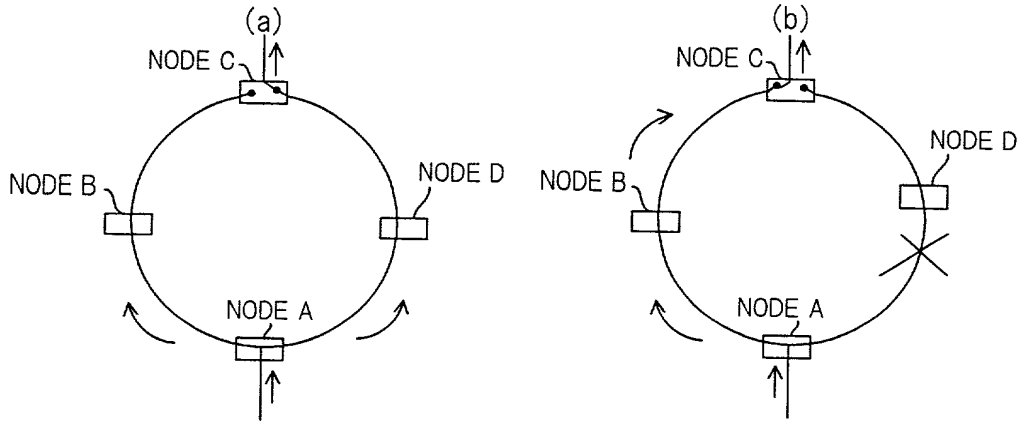

FIG. 20 PRIOR ART

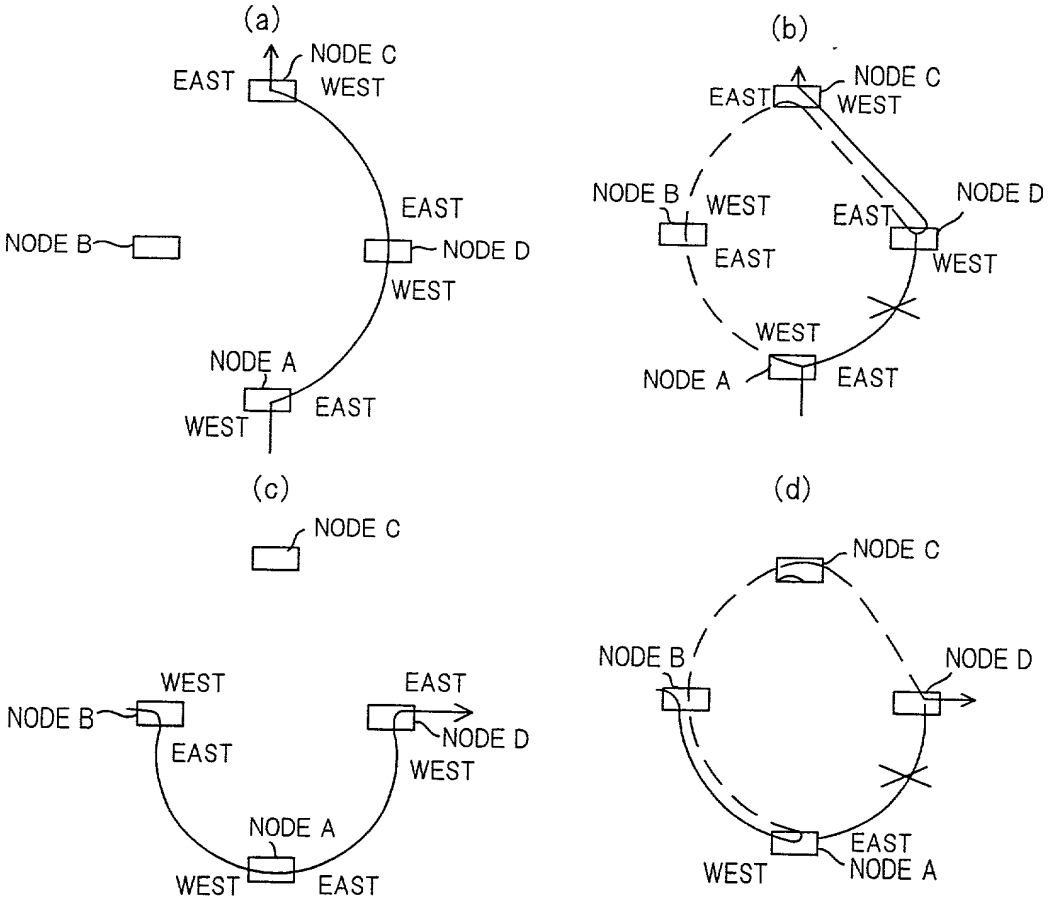

FIG. 21 PRIOR ART

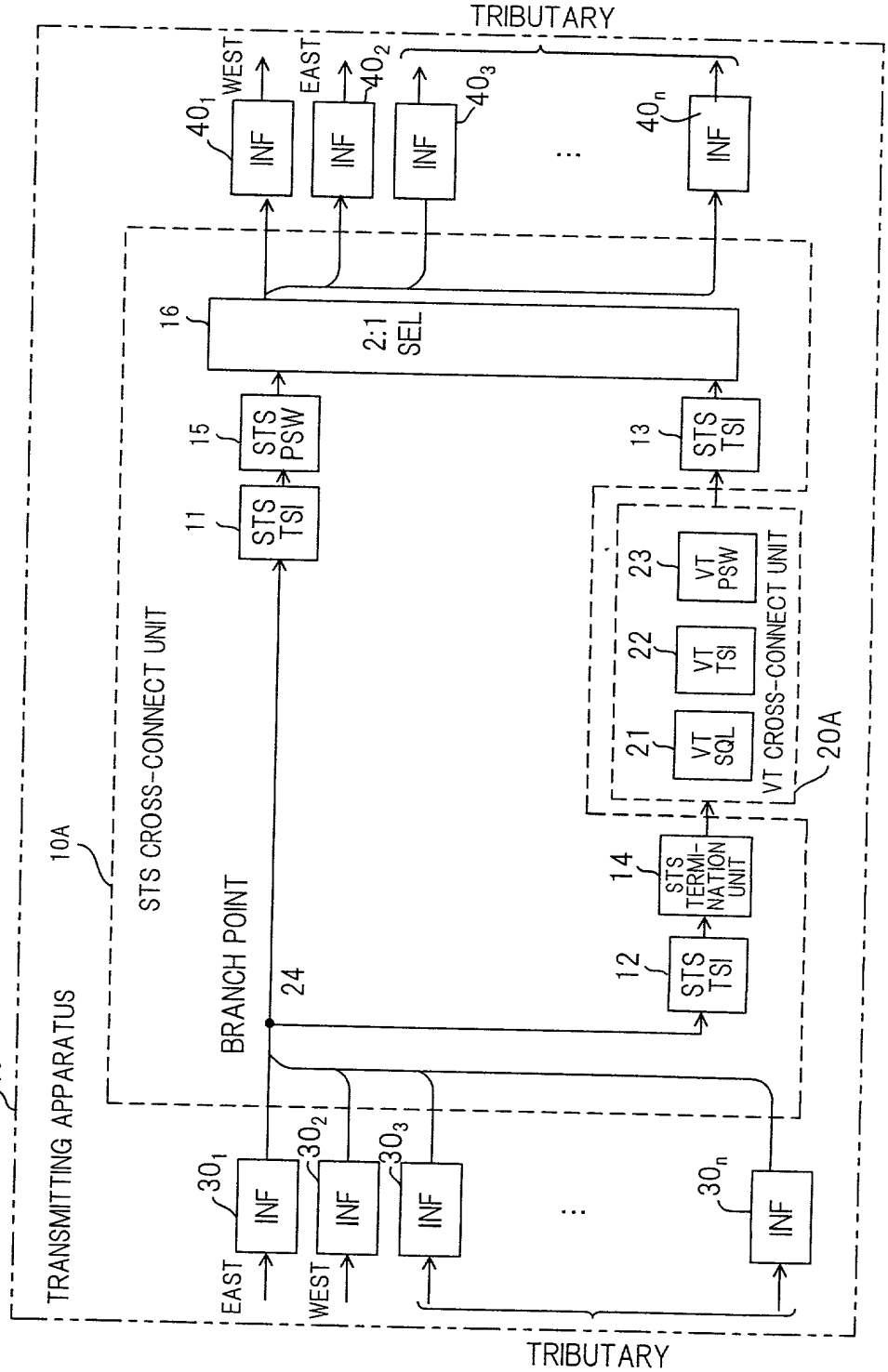

FIG. 22A PRIOR ART

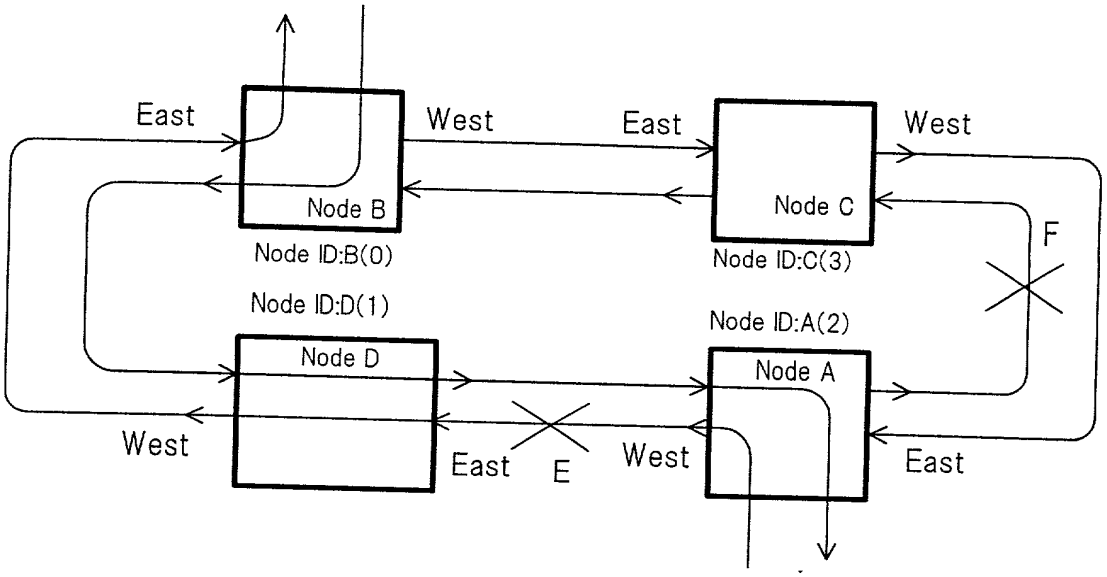

FIG. 22B PRIOR ART

Node B VT Squelch Table

East Side	West Side
2	0

FIG. 23 PRIOR ART

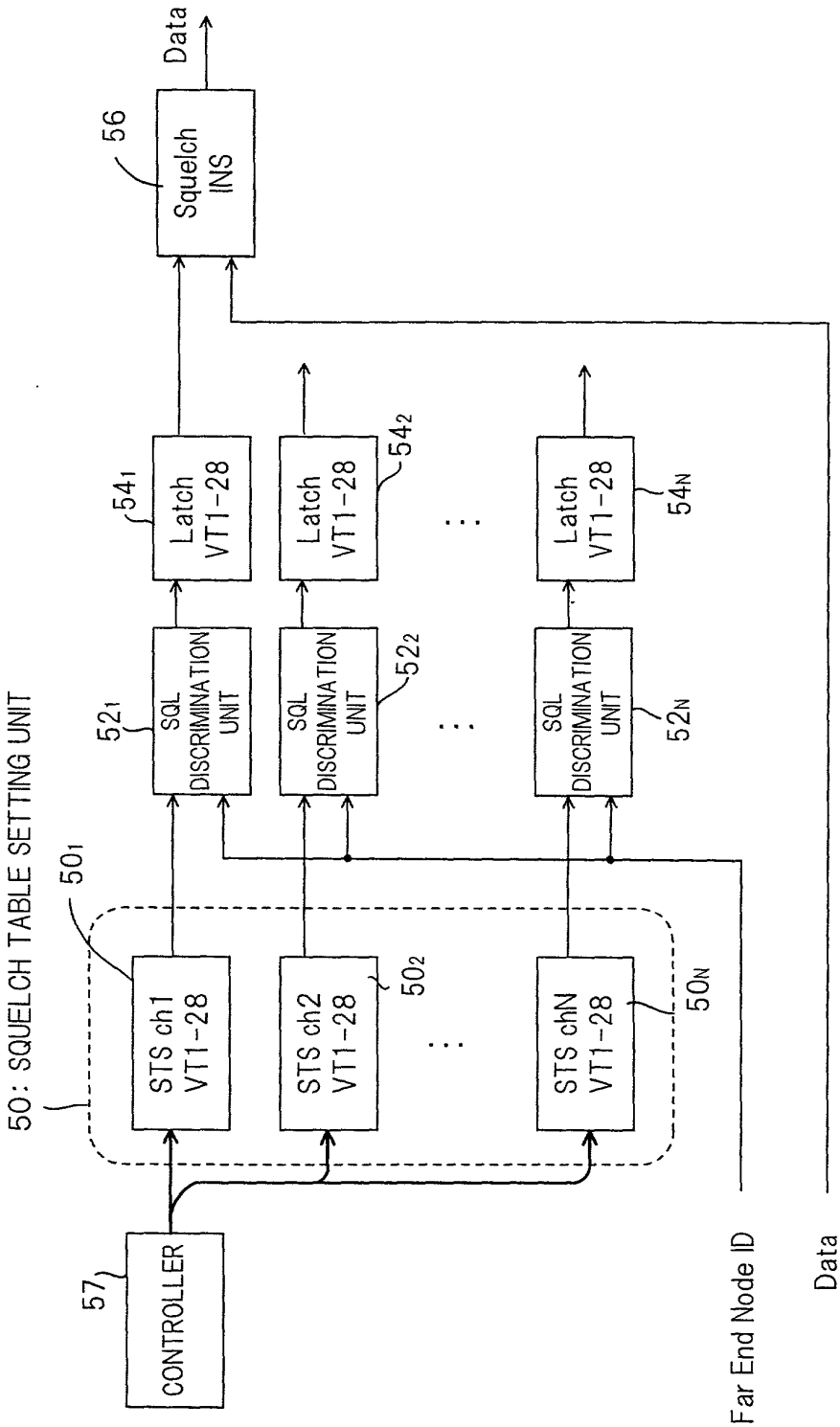

FIG. 24 PRIOR ART

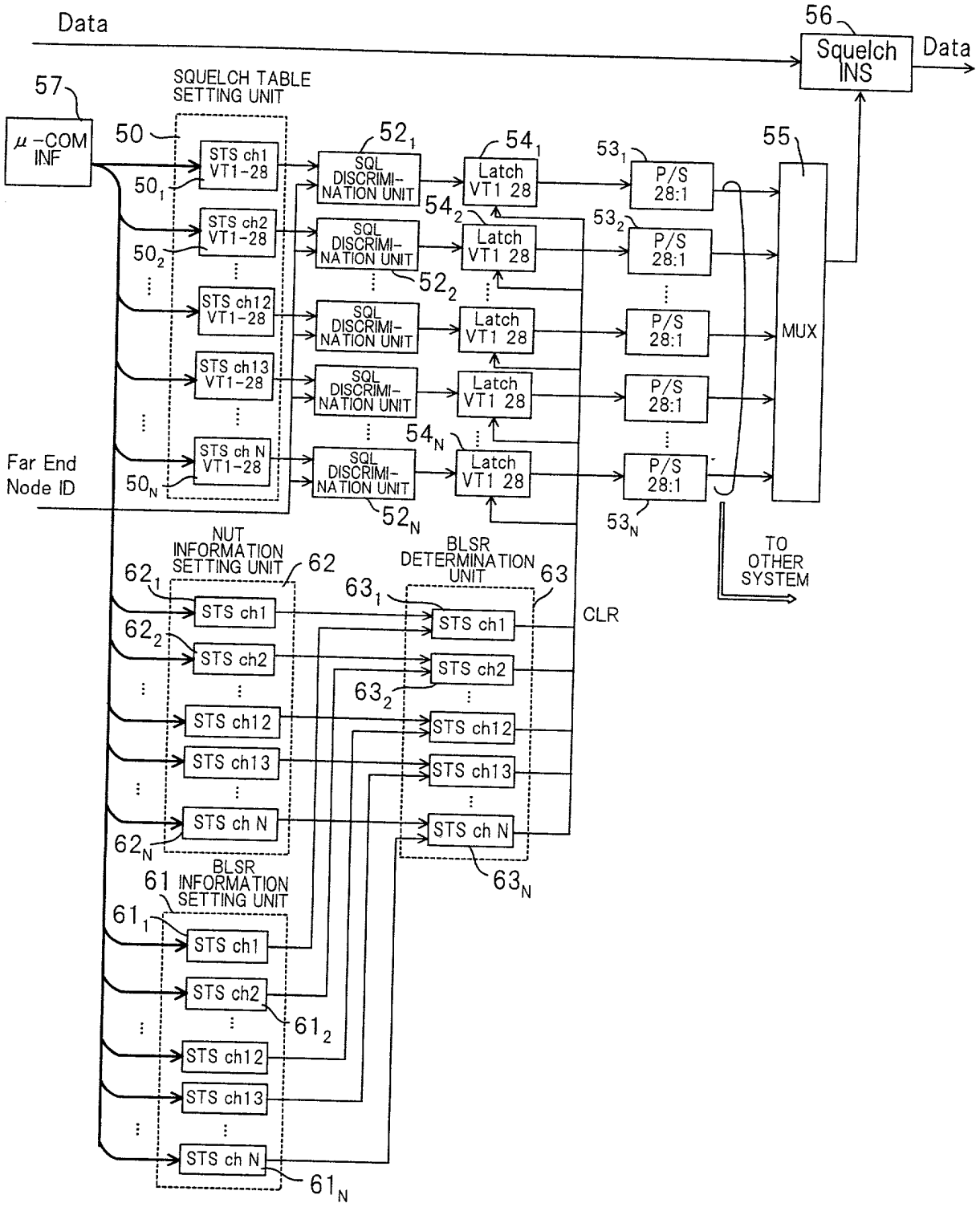

FIG. 25 PRIOR ART

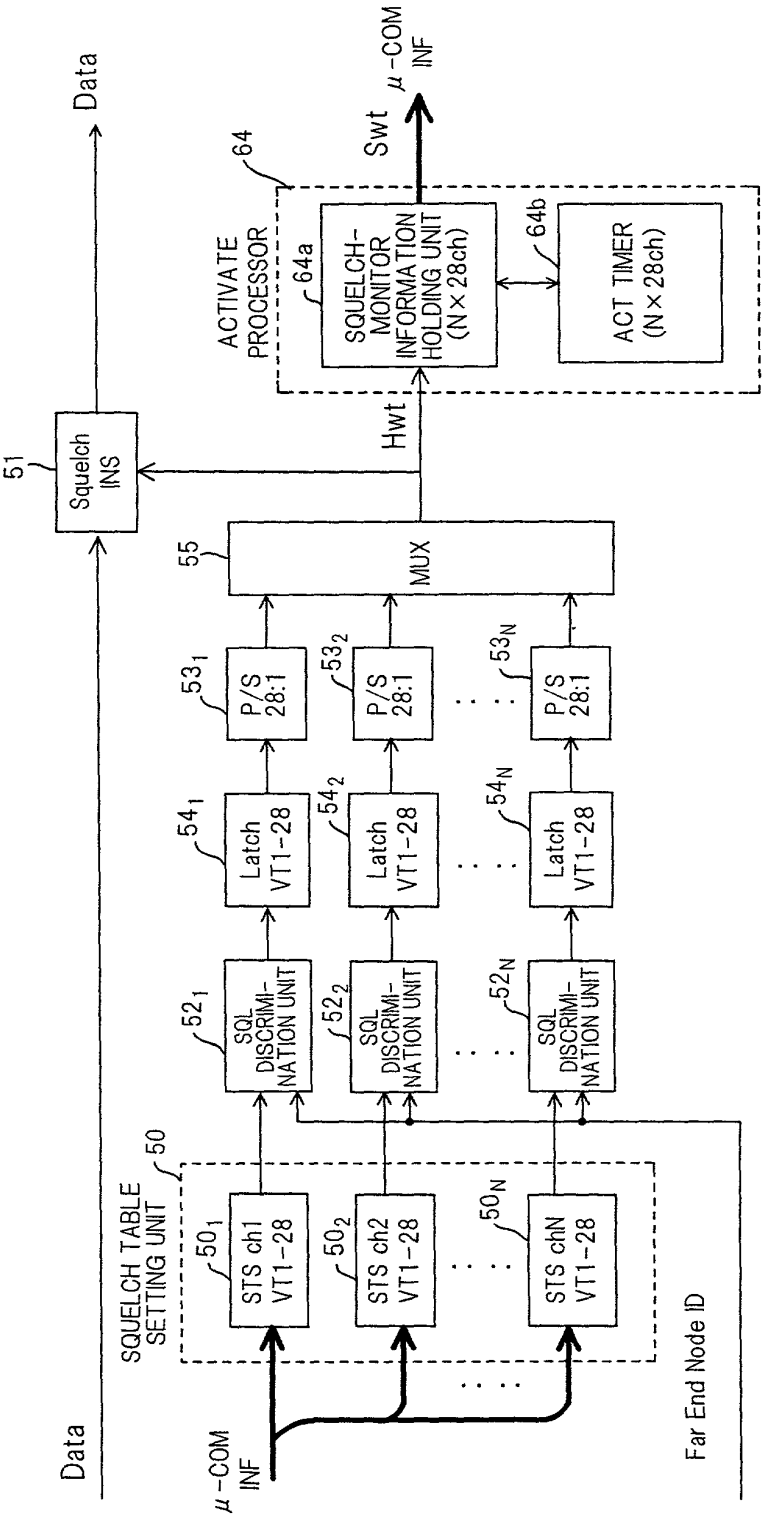

FIG. 26 PRIOR ART

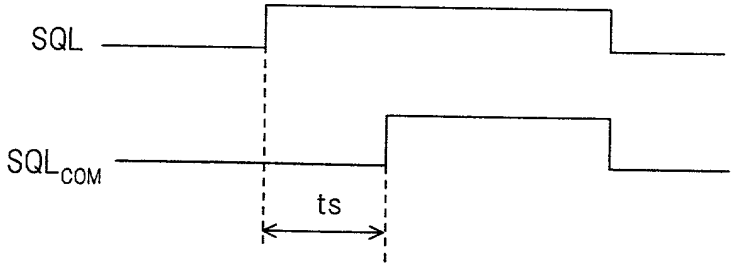

FIG. 27 PRIOR ART

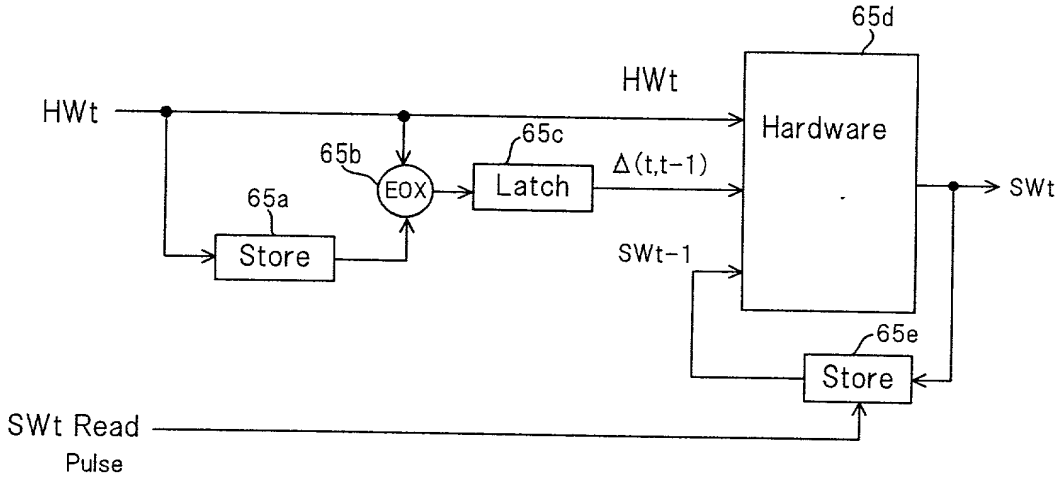

FIG. 28 PRIOR ART

SWt-1	Δ(t,t-1)	HWt	SWt
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

FIG. 29 PRIOR ART

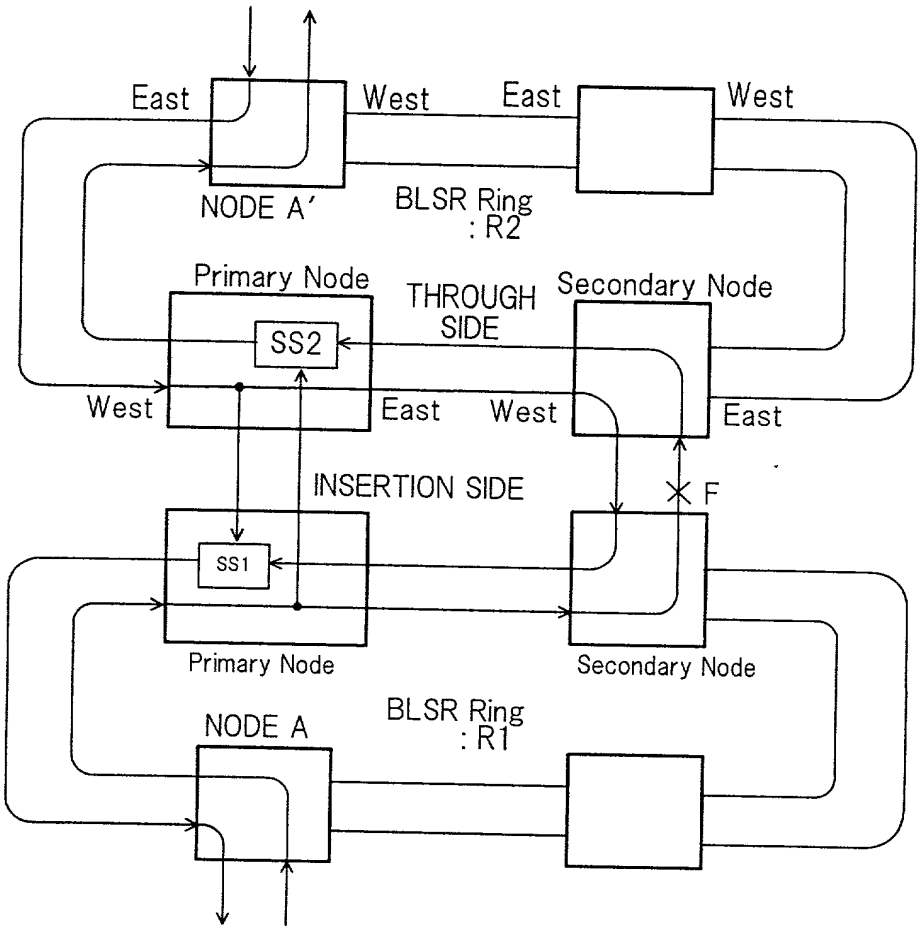

FIG. 30 PRIOR ART

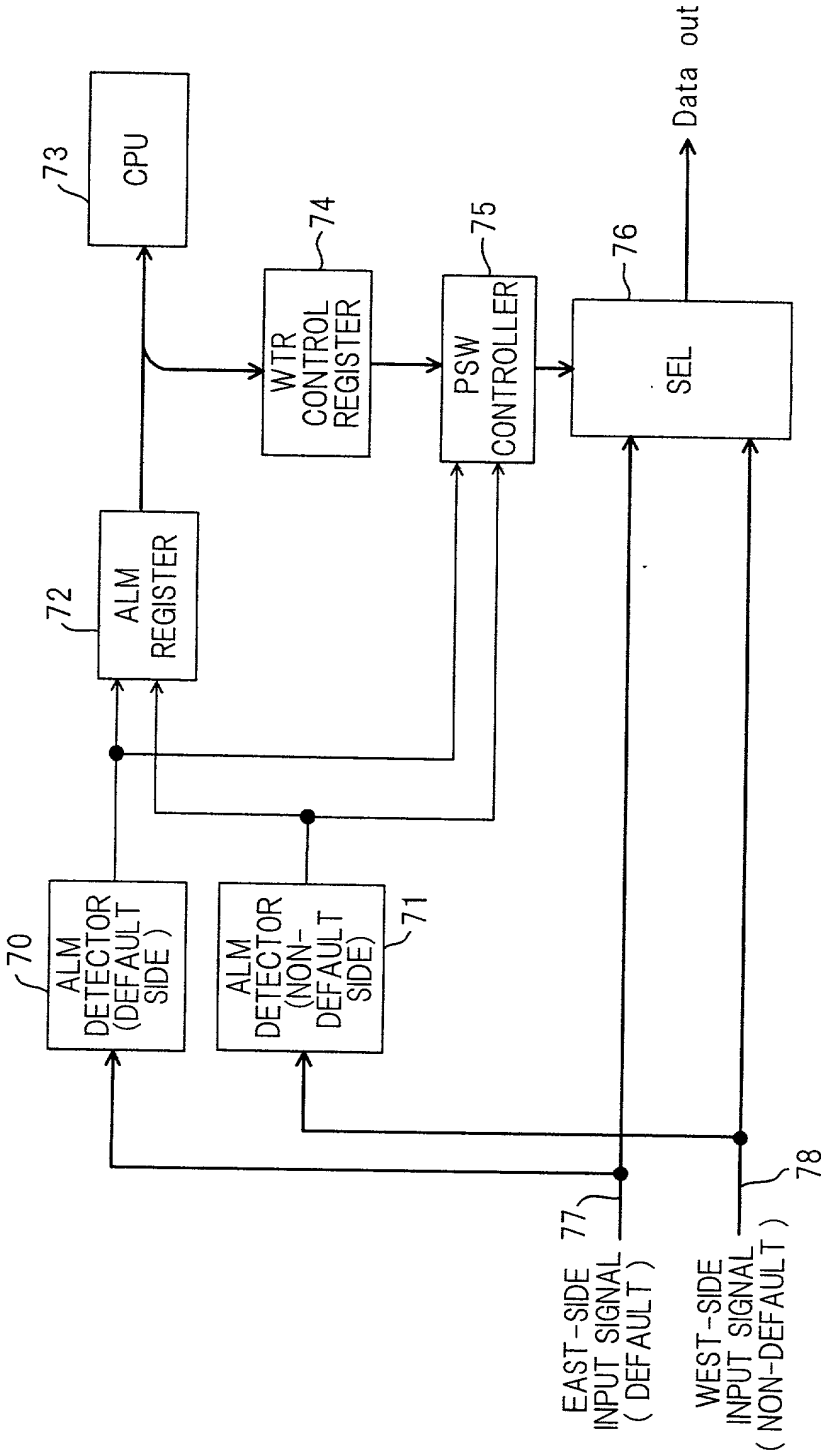

FIG. 31 PRIOR ART

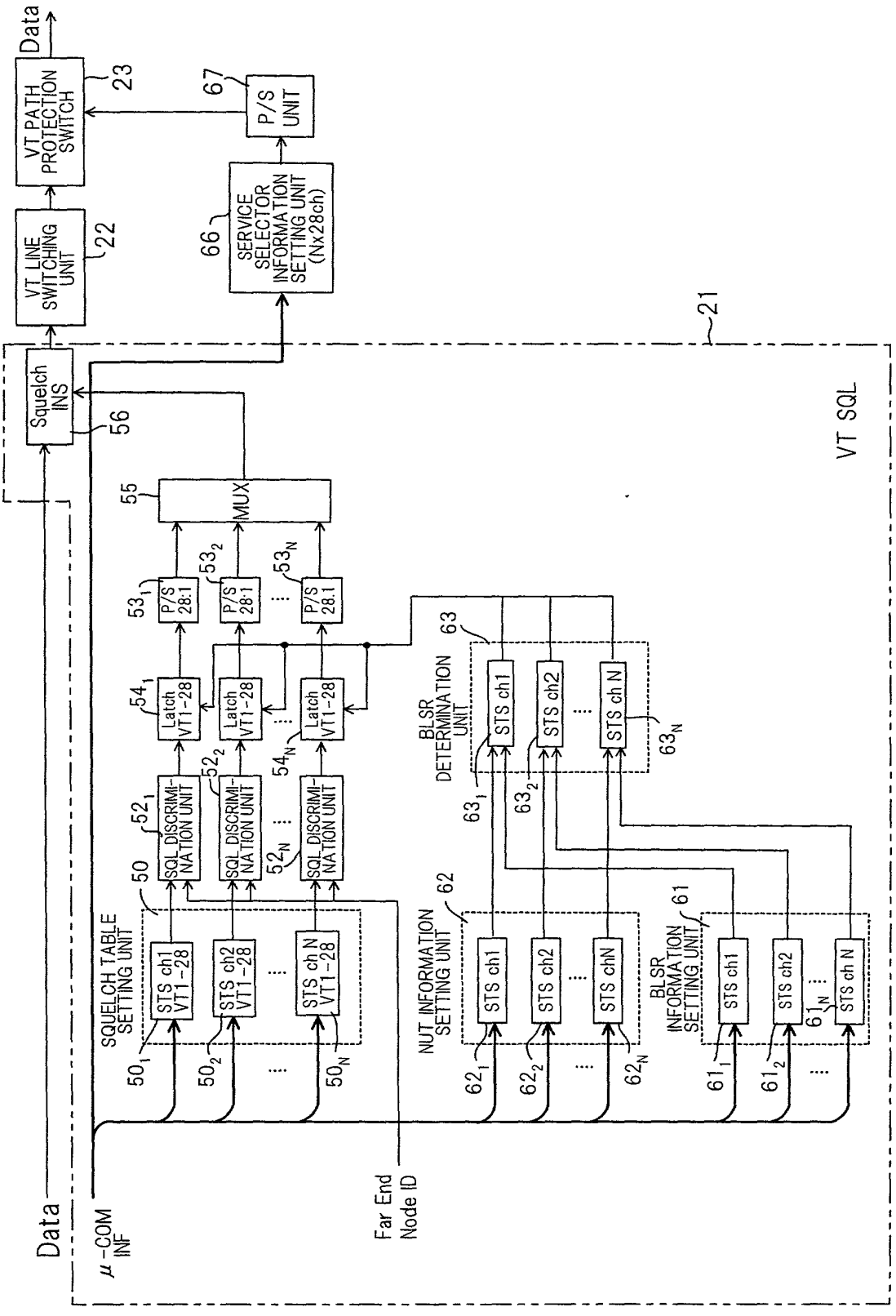
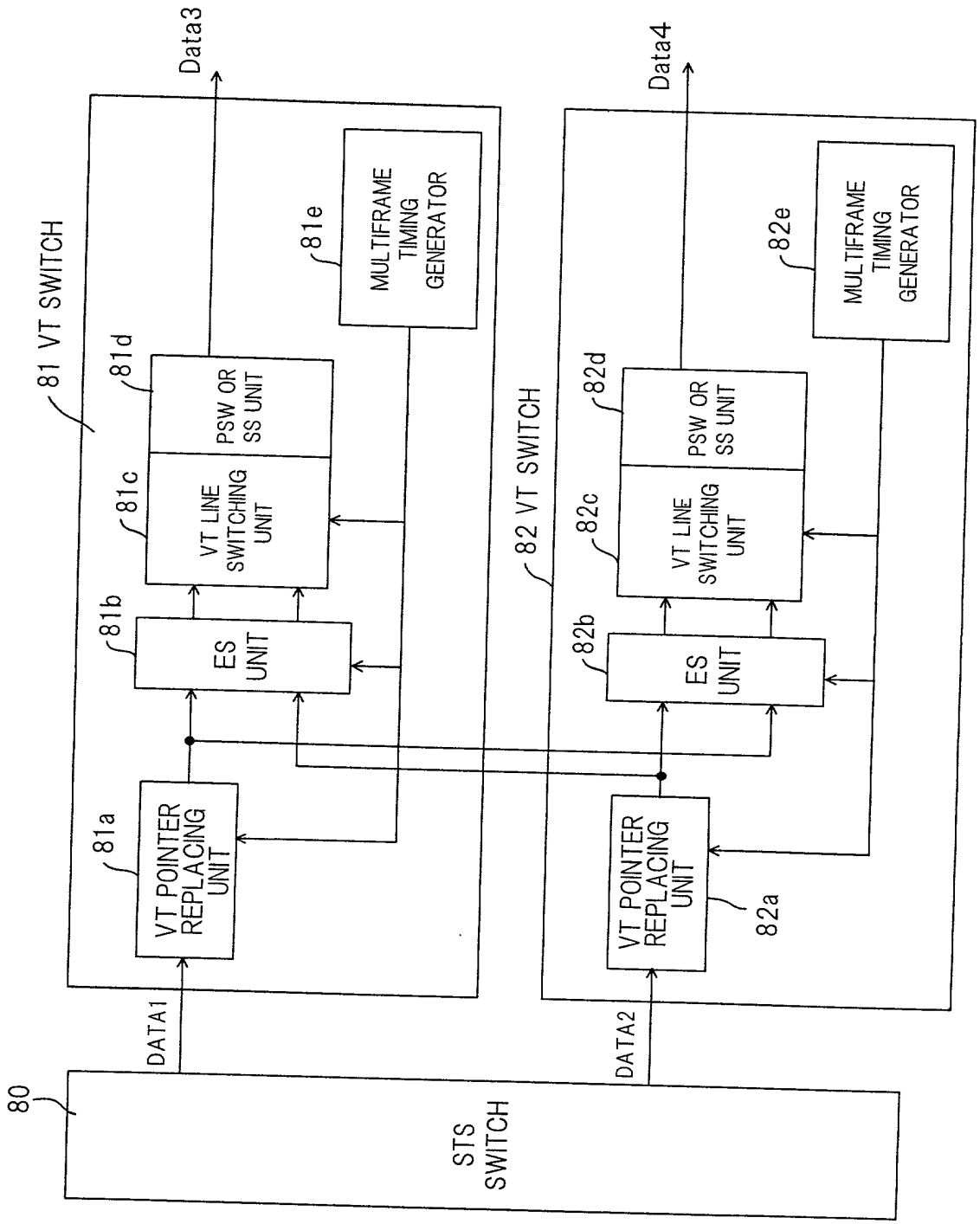
FIG. 32 PRIOR ART